Course: ECE 35800 - Introduction to VHDL

Type of Course: Required for CmpE Program, Elective for EE Program

Catalog Description: Introduction to the design of digital systems using VHDL hardware description language. Emphasis on how to write VHDL that will map readily to hardware. Projects assigned using commercial-grade computer-aided design (CAD) tools for VHDL-based design, VHDL simulation, and synthesis.

Credits: 3

Contact hours: 3

Prerequisite Courses: ECE 27000, CS 22900

Corequisite Courses: None

Prerequisites by Topics: Familiarity with the fundamentals of digital logic design – including combinational logic design, logic minimization, and state machine design; prior programming experience in a structured programming language highly desirable as preparation for learning to write VHDL code.


Course Objectives: At the end of this course, students should be able to:
- Code in VHDL for synthesis
- Decompose a digital system into a controller (FSM) and datapath, and code accordingly
- Write VHDL testbenches
- Synthesize and implement digital systems on FPGAs
- Understand behavioral, non-synthesizable VHDL and its role in modern design

Course Outcomes: Students who successfully complete this course will have demonstrated the ability to:
1. Understand and use major syntactic elements of VDHL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements. (a,k)
2. Design combinational logic in a variety of styles including: structural VHDL, and behavioral VHDL, as well as demonstrate an awareness of timing and resource usage associated with each approach. (a,c,k)
3. Create a VDHL test bench and use it to test/verify a sequential VHDL design of moderate complexity. (b,k)
4. Draw for a given commented VHDL code of moderate complexity, a corresponding RTL level block diagram. (a,b,k)

**Lecture Topics**

1. Course overview, VHDL synthesis and simulation design flow
2. Combinational logic design - schematic and VHDL
3. Use of test benches, timing constraints, optimization trade-offs
4. Sequential logic functions in VHDL
5. State machine design in VHDL
6. System level design in VHDL
7. Synthesis on FPGAs
8. Advanced VHDL topics

**Computer Usage**

High

**Laboratory Experience**

High

**Design Experience**

High

**Coordinator**

Guoping Wang, Ph.D.

**Date**

1/31/2017